Description

The TSSIXR28 SIP products using system-level packaging technology, integrated multi-gigasample RF data converter modules: include RF-ADCs 、 RF-DACs and soft-decision forward error correction(SD-FEC); integrated a feature-rich 64-bit quad-core ARM® Cortex™-A53 and dual-core ARM Cortex-R5 based processing system with 8GByte capacity on-chip DDR4-SDRAM external memory; integrated a large-scale programmable logic unit, also equipped with a 8GByte capacity on-chip DDR4-SDRAM external memory; integrated a 4Gb capacity QSPI NOR Flash used for system booting and configuration. All the resources above together form a powerful RF direct-sampling + processing micro-system in a single package. Greatly improve the density and flexibility of the system, at the same time, simplify the design、reduce design difficulty and shorten the product development cycle.

Features

- 8 channel RF-ADCs
  - 12-bit resolution;
  - Maximum sample rate: 4.096GSPS
  - Full complex mixers: 48-bit NCO per RF-ADC
  - direct-sampling RF capability
- 8 channel RF-DACs
  - 14-bit resolution
  - Maximum sample rate: 6.554GSPS
  - Full complex mixers: 48-bit NCO per RF-DAC
  - Up to 5GHz RF output
  - 4GHz full power output bandwidth
- Soft Decision Forward Error Correction (SD-FEC)
  - LDPCDecoding/Encoding
  - TurboDecoding
- Multi processor units
  - APU：64-bitquad-coreArmCortex-A53MPCores
    Operatingtargetfrequency:upto1.3GHz
    Single and double precision floating point operations
    32KB level 1 Cache
    1MBlevel2
    Cache
  - RPU：Dual-coreArmCortex-R5MPCores
    Operatingtargetfrequency:Upto600MHz
    Single and double precision floating point operations
    32KB level 1 Cache
  - Externalmemory：DDR4
    SDRAM 8GBytecapacity
    72bit width, ECC supported
- Feature-rich I/O Peripherals
  - PCIe：x1, x2, or x4 at Gen1 or Gen2 rates
  - SATA3.1：up to 6.0Gb/s data rates
  - USB3.0：2 controller, up to 5.0Gb/s data rates
  - SD/SDIO3.0：eMMC4.51 supported, HS200: up to 200MHz
  - UART：Programmable baud rate generator
  - CAN：Conforms to CAN2.0A and CAN2.0B standard, Bit rates up to 1Mb/s
- On-chip QSPI NOR FLASH
  - Forsystembootandconfiguration
  - 4Gbcapacity:2Gb*2pcs
- Programmable logic
  - Slice: 930,300
  - DSP Slice: 4,272
  - Block-RAM: 38Mb
  - PCIE: Gen3, 2channel
  - I/O: 143（High-Performance）
    48 (Hi-Range)
  - High-SpeedSerialTransceivers：GTY16channels
  - Externalmemorys：DDR4SDRAM
    8GBytecapacity
    72bit width, ECC supported
- Packaging and dimensions
  - BGA1760
  - 47.0mm*70.0mm

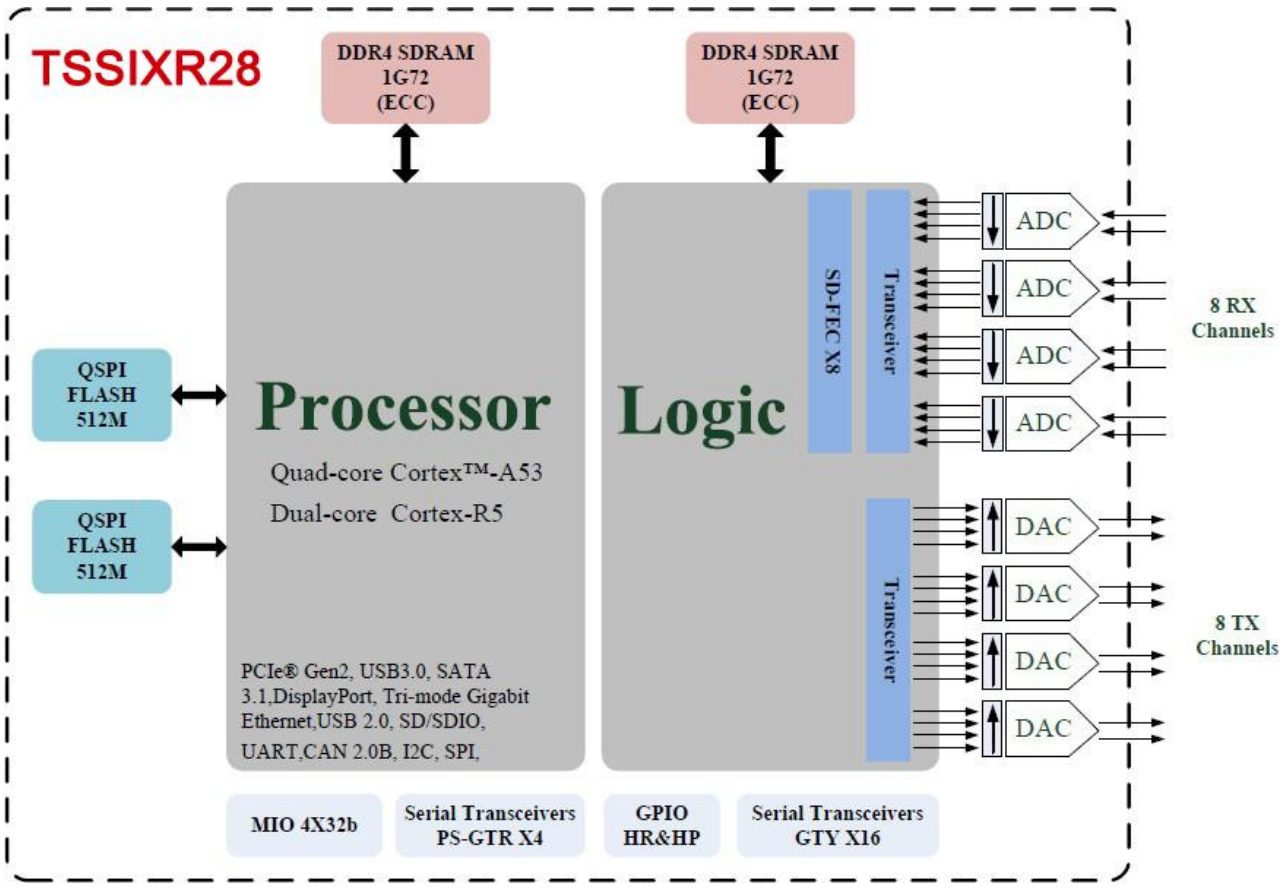
Benefits

- Compact package, 62% space savings in PCB area based on the same performance
- Simplify design, avoid complex and time-consuming PCB Layout
- work, accelerate product development processes
- Standardized、modular design, benefit upgrade and integration

Applications

- 5G and LTE Wireless
- Remote-PHY for Cable Access DOCSIS 3.1
- Phased Array Radar
- Satellite Communications
- Military Communications
- Test & Measurement
- LiDAR technologies

Figure 1 – Functional block diagram for TSSIXR28



NOTES: All passive components shown in the block diagram are included inside the 1670 BGA package,with essentially Decoupling Capacitors and Terminal Resistors in chip.

Development Kits

Xilinx Vivado Design Suite: System Edition,Version 2018.1 or later;

Xilinx SDK;

PetaLinux;

Ordering information